Curriculum Vitae

Dr. P SATISH KUMAR
Professor
Power Electronics and Drives, Multilevel Inverters, Renewable Energy Sources and
Hybrid Power Systems

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Department of Electrical Engineering, University College of Engineering, Osmania University, Hyderabad, Telangana State, INDIA – 500 007 email: satish_8020@yahoo.co.in	-

Academic Qualifications

- **Ph.D.** (Electrical Engineering), Jawaharlal Nehru Technological University Hyderabad, Hyderabad, 2011.
- **M.Tech.** (Power Electronics), Jawaharlal Nehru Technological University, Hyderabad, 2003.
- **B. Tech.** (Electrical and Electronics Engineering), Jawaharlal Nehru Technological University, Hyderabad, 1996.

Teaching Experience : 25 years

- **1996-2007** : Associate Professor, Private Engineering Colleges, Affiliated to JNTU, Hyderabad.
- **June 2007 - June 2015** : Assistant Professor,University College of Engineering, Osmania University, Hyderabad.
- **June 2015 - June 2018** : Associate Professor,University College of Engineering, Osmania University, Hyderabad.
- **June 2018 - Till date** : Professor,University College of Engineering, Osmania University, Hyderabad.

Research

Projects

1. **Indo – Sri Lanka Joint Research Project:** "Design and Development of Hybrid Wind-Solar Power Generation System using Multilevel Inverters for Grid Connected Applications", Principal Investigator: **Dr. P. Satish Kumar**, Project Cost: Rs.25,99,780/-. Duration of Project: 3 years, Sponsored by the Department of Science and Technology (DST), New Delhi **(On-Going).**
2. **UGC-Major Research project** on Cascaded H-bridge Multilevel Inverters, Principal Investigator: **Dr.**

P. Satish Kumar, Project Cost: Rs. 8, 49, 000/-, Duration of Project: 3 years, Sponsored by the University Grants Commossion (UGC), New Delhi **(Completed)**.

3. **SERB (DST) - Research Project** on Neutral point clamped Multilevel Inverters, Principal Investigator: **Dr. P. Satish Kumar,** Project Cost: Rs. 20, 10, 000/-, Duration of Project: 3 years, Sponsored by the Science and Engineering Research Board (SERB), New Delhi **(Completed).**

Patents:

1. **Australain Innovation Patent** granted on "Machine Learning Based Fish Monitoring Machine and Method Thereof", Patent number: 2020102433, Published in IP Australia on 25/09/2020.
2. **Design Patent** granted on "Smart Self Disinfecting Face Shield", Design No. 330167-001, dated 18-06-2020 by Intellectual Property India, The Patent Office, Certificate of registration of design, Government of India.
3. Filed a **Patent** on "Implementation of SVPWM Techniques to A Multilevel Inverter", Application No. 201741042315A, Published in the Official Journal of Patent, Issue No. 48/2017, page No. 45227, dated 01/12/2017.
4. Filed a **Patent** on "Asymmetrical Cascade H-Bridge Multilevel Inverter with Reduced Power Switches", Application No. 201741033742A, Published in the Official Journal of Patent, Issue No. 09/2018, page No. 7745, dated 02/03/2018.
5. Filed a **Patent** on "Novel Interline Unified Power Quality Conditioner (IUPQC) for Multi-feeder system with four converters". Application No. 201941045730, published in the Official Journal of Patent, Issue No. 35/2020, page No. 34715, dated 28/08/2020.
6. Established **"Research Lab for Multilevel Inverters"** in the Department of Electrical Engineering, University College of Engineering, OU as a part of two major research projects sponsored by UGC and SERB, New Delhi in the year 2014. Five Research scholars already obtained thier PhD degrees from this Research Lab and eight research scholars are utilising the lab to carry out their research work.

List of model / prototype / demonstration units created for display/deployment

1. Three phase Eleven level cascaded H-bridge Inverter, 2015.
2. Three Phase Seven-Level Neutral Point Clamped Inverter, 2016.
3. Asymmetrical Cascaded H-bridge Seven-Level Inverter with Reduced Power Switches, 2017.

Ph.D. Scholars under my Guidance
No. of PhD's Awarded: 05

1. **Mrs. B. Sirisha :** Ph.D. thesis entitled "Optimal Space Vector Pulse Width Modulation Methods for Cascaded H- Bridge and Diode Clamped Multilevel Inverters Including Over Modulation Region", May 2018.
2. **Mrs. N. Susheela:** Ph.D. thesis entitled "Implementation and Analysis of Various Pulse Width Modulation Control Strategies for Diode Clamped Multilevel Inverter and Hybrid Multilevel Inverter Topologies", August 2018.
3. **Mr. Ch. Lokeshwar Reddy** : Ph.D thesis entitled "Investigation and Implementation of Control Strategies for Multilevel Inverters", December 2018.
4. **Mr. G. Sridhar:** Ph.D. thesis entitled "Design and Implementation of A Novel Topology for Cascaded H-Bridge Multilevel Inverter with Reduced number of Switches", August 2019.

5. **Mr. Thota Surya Prakash:** Ph.D. thesis entitled "A Novel Four Converter Topology of Interline Unified Power Quality Conditioner for Power Quality Improvement in Multi-Feeder Systems", March, 2021.

No. of PhD's guiding: 08

Seminars Organized

1. **Coordinator**: A Training Programme on 'Implementation of space vector pulse width modulation for multilevel inverters using FPGA' is conducted in the Research Lab, Dept. Of Electrical Engineering, UCE, OU on 16th and 17th September, 2016.
2. **Coordinator**: A National Level Technical Symposium "Techsonance-2015", organized by the Department of Electrical Engineering, UCE, OU in the year 2015.
3. **Coordinator**: One Week Faculty Development Programme on "Advances in Power Electronics and Drives" organized by the Department of Electrical Engineering, UCE, OU, during 12th–17th May, 2014.
4. **Coordinator**: Continuing Professional Development Programme on "Recent Trends and Practical Applications of Power Electronics in Power Systems" organized by the *Engineering Staff College of India,* Hyderabad, during 28th–31st January 2014.
5. **Coordinator**: A National Level Technical Symposium "Techsonance-2011", organized by the Department of Electrical Engineering, UCE, OU during 25th–26th March 2011.
6. **Coordinator**: One day workshop on "Technical & Personality Skills for Electrical & Electronics Engineering" organized by the Department of Electrical Engineering, UCE, OU in collaboration with SMS Educational Society, Hyderabad on 28th March 2009.

Others

- **Countries visited for Joint Research Projects/ International Conferences:** United States of America, Singapore, Hong Kong, Paris, Switzerland, Bangkok, Sri Lanka and Japan.

Awards / Honours / Achievements

Awards

1. Received **"Best Teacher Award-2014"** from the State Government of Telangana, on 5th September, 2014.
2. Received "**Certificate of Merit**" for the presentation of research paper in the "International Conference on Electrical Engineering and Applications 2013", University of California, San Francisco, USA.
3. Received "**Fast Track Scheme for Young Scientist Award**" from the Science and Engineering Research Board (SERB), New Delhi, in the year 2013.
4. Received **"Award for Research Excellence-2014"**.
5. Received **"Global Teacher Role Model Award-2015"**.
6. Received **"Certificate of Excellence"** for the presentation of research paper in the International Conference on Emerging Trends in Electronics, Electrical and Mechanical Engineering (ICEEME-2018) held at Bhopal, India.

Honours

- Member, Board of Studies in Electrical Engineering, Kakatiya University, Warangal (2020- Till date).

- Member, Board of Studies in Electrical Engineering, Chaitanya Bharathi Institute of Technology, Hyderabad (2021- Till date).

Achievements

Research Activates / International visits:

- Visited **University of Moratuwa, Sri Lanka** in Feb 2019 on their invitation to discuss the recent trends in research and development in the area of electrical engineering, interacted with faculty members and visited research laboratories.
- Visited Electrical Machines and Drives Laboratory, **National University of Singapore (NUS), Singapore** and interacted with faculty, research fellows and PhD students, discussed various research topics and explained them the various topologies of multilevel inverters.
- Visited Research Lab for Power Electronics, **Nanyang Technological University (NTU), Singapore** and made many useful discussions on the Laboratories, Research and Multilevel Inverters.
- Visited **University of Ruhuna, Sri Lanka** and developed prototype of Hybrid Power System in the department of Electrical & Information Engineering, Ruhuna University.
- **Session Chair**: International Conference on Electrical Engineering and Applications 2013, The world Congress on Engineering and Computer Science 2013, San Francisco, USA, 23- 25 October, 2013.
- Delivered **Keynote address** in "International Conference on Electrical Engineering: Theory and Application-2014", Singapore.
- **Session Chair:** International Conference on Electrical Engineering: Theory and Application (ICEETA 2014), 30-31 March, 2014, Singapore.
- **Session Chair:** International Conference on Engineering, Science, and Industrial Applications (ICESI), Aug. 22-24, 2019, at Tokyo University of Science, Tokyo, Japan.
- Visited USA, Paris, Switzerland, Singapore, Bangkok, Hong Kong and Sri Lanka to present research papers in various International Conferences and to engage in research activities.
- Delivered expert lectures in reputed organizations like Academic Staff College, Universities, Engineering Staff College of India, National Institute of Science and Technology, Engineering Colleges, Research Institutes and various Organizations.

Administrative Experience

- Additional Controller (Confidential), Examination Branch, Osmania University (2021 - Till date).
- Chairperson, Board of Studies in Electrical Engineering, Osmania University (2019 - Till date).
- Director, Diamond Jubilee Library, University College of Engineering, OU (2020 - Till date)
- Chairperson, Board of Studies in Electrical Engineering, UCE (A), OU (March 2019 - 2020).
- Additional Controller (Confidential), Examination Branch, Osmania University (2015 - 2019).
- Joint Director of Evaluation, UCE, OU from 2012 to 2014.
- Warden, Kinnera Hostel, UCE, OU from 2009 to 2016.
- In charge-Examinations, Department of Electrical Engineering, UCE, OU for one year.
- Faculty Adviser, E., Power Electronic Systems, UCE, OU for one year (2013-2014).
- Faculty Adviser, M., Industrial Drives and Control, UCE, OU from 22nd June 2009 to 2013.
- Member: Student Activities Board (Hostels & Messes), UCE, OU (2009- 2017).
- Member: Anti Ragging Committee, UCE, OU (2009- 2017).
- Member: Anti Ragging Squads (Hostel & Transport), UCE, OU (2009- 2017).
- Advisory Board Member: Engineering Staff College of India, Hyderabad.

- Coordinator: PGECET 2012, Conducted by Osmania University.
- Convener: ME PTPG Admissions 2012, Department of Electrical Engineering, UCE, OU.
- Regional Coordinator: Conducting of PGECET- 2013 in Hyderabad region.
- Regional Coordinator: Conducting of PGECET- 2014 in Hyderabad region.
- Subject expert for preparing Question bank for Examination of the subject "Electrical Circuits" for JNTUH, Hyderabad.
- Member: Syllabus review of electrical engineering subjects for Polytechnic colleges.
- Member: Syllabus review of electrical engineering subjects for Polytechnic colleges.
- Advisory Board Member: Engineering Staff College of India, Hyderabad.

Workshops/ Faculty Development Programmes Attended

1. Two day Workshop on 'Academic Administrators' organised by the UGC- Human Resource Development Centre (Academic Staff College), Osmania University, Hyderabad during 29-30 June 2018.
2. One Week Faculty Development Programme on "Distributed Generation and Power Quality Issues" conducted by Department of Electrical Engineering, UCE, OU during 30th June – 5th July 2014.
3. One Week Faculty Development Programme on "Recent Advances in VLSI" conducted by Department of ECE, UCE, OU during 09-14 June 2014.
4. Two Week "Faculty Development Programme in Entrepreneurship" Sponsored by NSTEDB DST, New Delhi conducted by Entrepreneurship Development Cell, OU during 01-15 June 2011.
5. Three Week UGC Sponsored Refresher Course on "Advances in Power Electronics and Electric Drives" conducted by UGC-Academic Staff College, JNTUH, Hyderabad from 09th - 28th of August 2010.
6. Orientation Programme organised by Osmania University Centre for International Programmes, Osmania University during 02-12 July 2007.
7. Three Week UGC Sponsored Refresher Course on "Simulation Tools for Electrical Engineering Applications" conducted by UGC-Academic Staff College, JNTUH, Hyderabad from 06th - 25th of December 2004.
8. Four day Training Programme on "Advanced Digital Design using Verilog HDL" conducted by MVSR Engineering College, Hyderabad during 28-31 Jan 2015.
9. Short Term Course on "Energy Management and Resources", conducted by National Institute of Technical Teachers Training and Research, Chennai during 12-16 December 2011.
10. Short Term Course on "Micro Controller and Its Applications", conducted by National Institute of Technical Teachers Training and Research, Chandigarh during 23-27 May 2011.
11. One week AICTE Sponsored Staff Development Programme on "Recent Trends in Electrical Drives and Power Electronics" Conducted by National Institute of Science and Technology, Berhampur during 12-17 Oct, 2009.
12. National Level Workshop on "Advances in Power Electronics and Drives", conducted by Pulla Reddy Engineering College during 27-28 Dec, 2008.
13. A Workshop on "EDSA Software Application to Power Systems" conducted by Department of Electrical Engineering, University College of Engineering, Osmania University, Hyderabad during 05-06 Dec, 2008.
14. Workshop on "Modelling, Simulation and Control of Power Converters" Conducted by Department of Electrical Engineering, NIT, Warangal during 09-13 June 2008.
15. Workshop on "Developments in Power, Power Electronics and Drives" Conducted by Vasavi

College of Engineering, Hyderabad during 10-11 March, 2008.

16. Three day Workshop on "Embedded Systems Design with 8051 Micro Controller" Conducted by Wine Yard Technologies, Hyderabad during 30th Nov – 02nd Dec 2007.

17. A Workshop on "Power Quality" conducted by Department of Electrical Engineering, University College of Engineering, Osmania University, Hyderabad during 28-29 Sep, 2007.

18. Two day National Level Workshop on "Recent Trends in Power Electronics and Drives", conducted by G. Pulla Reddy Engineering College during 08-09 Feb, 2007.

Memberships in Professional/Scientific Bodies

1. Secretary: IEEE PES/ IAS/ PELS Society Joint Chapter, IEEE Hyderabad Section.
2. Senior Member: IEEE Industry Applications Society.
3. Fellow of Institute of Engineers (FIE).
4. Life Member: Indian Society for Technical Education (ISTE).
5. Life Member: System Society of India (SSI).
6. Life Member: International Association of Engineers (IAENG).
7. Life Member: International Association of Computer Science and Information Technolog
8. Life Member: Engineering and Scientific Research Groups (ESR Group).
9. Life Member: World Academy of Science, Engineering and Technology (WASET).
10. Life Member: International Congress for Global Science and Technology (ICGST).

Editorial Board Member:

1. Journal of Electrical Electronics Engineering Research.
2. Journal of Engineering, Technology& Applied Science Research.
3. International Journal of Power Electronics and Drive Systems.
4. International Journal of Engineering and Advanced Technology.
5. Journal of Bulletin of Electrical Engineering and Informatics.

Reviewer for International Journals:

1. IEEE Transactions on Power Electronics.
2. IEEE Access Journal.
3. IETE Journal of Research, Taylor and Francis Publications.
4. International Transactions on Electrical Energy Systems, Wiley Publications.
5. International Journal of Ambient Energy, Taylor and Francis Publications.

List of Publications

Peer-Reviewed Papers

No. of Publications : 100 (International Journals: 63; Conferences : 37)

1. T. Surya Prakash, P. Satish Kumar, R. P. S. Chandrasena, "A Novel IUPQC for Multi-Feeder Systems using Multilevel Converters with Grid Integration of Hybrid Renewable Energy System" IEEE Access Journal, Vol. 8, pp. 44903– 44912, March 2020.

2. P. Satish Kumar, R. P. S. Chandrasena, V. Ramu, G. N. Srinivas, K. Victor Sam Moses Babu, "Energy Management System for Small Scale Hybrid Wind Solar Battery Based Microgrid" IEEE Access Journal, Vol. 8, pp. 8336 – 8345, January 2020.

3. Susheela, P.Satish Kumar, S.K.Sharma, "Generalized Algorithm of Reverse Mapping Based SVPWM Strategy for Diode Clamped Multilevel Inverters", IEEE Transactions on Industry Applications, Vol. 54 , Issue: 3 , pp. 2425-2437, May-June 2018.

4. P. Satish Kumar, R.P.S. Chandrasena and K. Victor Sam Moses Babu, "Design and Implementation of Wind Turbine Emulator using FPGA for Stand Alone Applications" International Journal of Ambient Energy (Taylor and Francis Publications), March 2020.

5. Surya Prakash Thota, Satish Kumar Peddapelli "A New Topology of Interline Unified Power-Quality Conditioner for Multi Feeder System"Learning and Analytics in Intelligent Systems (Springer Publications), Vol. 4, pp. 507–519, 2020.

6. B. Sirisha, P. Satish Kumar "A Simplified and Generalised SVPWM Method Including Over Modulation Zone for Seven Level Diode Clamped Inverter – FPGA Implementation" International Journal of Power Electronics, (Inderscience Publications), Vol.10 No.4, pp. 350–366, 2019.

7. Ch. Lokeshwar Reddy, P. Satish Kumar, M. Sushama "Implementation and Performance Analysis of Cascaded Multilevel Inverter using Modified SVPWM Techniques" *International Journal of Power Electronics* (Inderscience Publications). vol.9, no. 3, 2018.

8. Ch. Lokeshwar Reddy, P. Satish Kumar, M. Sushama "Design and Performance Analysis of Seven-Level Diode Clamped Multilevel Inverter using Modified SVPWM Techniques" *International Journal of Engineering,* vol.30, no. 11, November 2017.

9. Susheela and P.Satish Kumar, "Performance Analysis of FPGA based Diode Clamped Multilevel Inverter Fed Induction Motor Drive using Phase Opposition Disposition Multicarrier Based Modulation Strategy", International Journal of Power Electronics and Drive Systems, ISSN: 2088-8694, Vol.8, No.4, pp.1512- 1523, December 2017.

10. Susheela and P.Satish Kumar, "Performance Evaluation of Multicarrier Based Techniques for Single Phase Hybrid Multilevel Inverter using Reduced Switches," Indonesian Journal of Electrical Engineering and Computer Science, Vol. 7, No. 3, pp. 676-686, September 2017.

11. Susheela and P.Satish Kumar, "Comparative Analysis of Carrier Based Techniques for Single phase Diode Clamped MLI and Hybrid Inverter with Reduced Components," Indonesian Journal of Electrical Engineering and Computer Science Vol. 7, No. 3, pp. 687 – 697, September 2017.

12. Susheela and P.Satish Kumar "Analysis and Comparison of Various Pulse Width Modulation Strategies for Hybrid Inverter with Reduced Number of Components," International Journal of Inventions in Engineering & Science Technology (IJIEST), e-ISSN:2454-9584; p-ISSN: 2454-8111, Vol. No. 3, pp.12-26, Jan-Dec 2017.

13. Susheela and P.Satish Kumar "Evaluation of Carrier Based Neutral Point Potential Regulator with Small DC Link Capacitors for Diode Clamped Inverter," International Journal of Inventions in Electronics & Electrical Engineering (IJIEEE), e-ISSN: 2454-9592; p-ISSN: 2454-8081, Vol. No. 3, pp.9-22, Jan-Dec 2017.

14. Sridhar, P. Satish Kumar, M. Sushama "Phase Disposition PWM Techniques for Eleven level Cascaded Multilevel Inverter with Reduced number of Carriers" in *Asian Power Electronics Journal (APEJ)*, Vol. 11, No. 1, July 2017, pp.1-5.

15. Susheela and P.Satish Kumar, "Performance Evaluation of Carrier Based PWM Techniques for Hybrid Multilevel Inverters with Reduced Number of Components," Energy Procedia Volume 117, pp. 635-642, June 2017.

16. Sridhar, P. Satish Kumar, M. Sushama " A Novel Generalised Topology for Multilevel Inverter with Switched Series-Parallel DC Sources" in *International Journal of Engineering (IJE) TRANSACTIONS C : Aspects*, Vol. 30, No. 6, June 2017, pp. 851-858.

17. Ravi Kumar Bhukya, Satish Kumar, "Performance Analysis of Modified SVPWM Strategies for Three Phase Cascaded Multilevel Inverter fed Induction Motor Drive", *International Journal of Power Electronics and Drives Systems,* Vol 8, No 2, pp. 835-843, 2017.

18. Ch. Lokeshwar Reddy, P. Satish Kumar, and M. Sushama, " Design and Performance Analysis of Cascaded H-Bridge Multilevel STATCOM" *International Journal of Control Theory and Applications*, vol. 10, no. 16, pp. 1-11, 2017, ISSN: 0974-5572.

19. Ch. Lokeshwar Reddy, P. Satish Kumar, M. Sushama "Performance Comparison of Star Connected Cascaded STATCOM for Different PWM Techniques" *International Journal of Power Electronics and Drive Systems,* vol. 8, no. 3, 2017.

20. Bogimi Sirisha, P. Satish Kumar , "A Simplified Space Vector Pulse Width Modulation Method Including Over Modulation Operation for Five Level Cascaded H-bridge Inverter with FPGA Implementation", International Journal of Power Electronics and Drives Systems (IJPEDS), Vol 8, No 3, September 2017. Pp.1203-1211 (ISSN: 2088-8694, doi: 10.11591/ijpeds.v8.i3) (SJR 0.25) (H index 9) (Scopus indexed).

21. Sirisha, P.Satishkumar" Space Vector Pulse Width Modulation Technique for Five Level Cascaded H-Bridge Inverter Including Over Modulation Region", *International Journal of Inventions In Electronics & Electrical Engineering* Vol 2, December 2017.(ISSN NO:2347-6982),(Impact factor:2.51).

22. Ravi Kumar Bhukya, Satish Kumar "Modeling, Analysis and Comparative of Down Sampling Based Clamping SVPWM for Cascaded and Diode Clamped Multilevel Inverter fed Induction Motor Drive", Indonesian Journal of Electrical Engineering and Computer Science, Vol. 7, No. 3, September 2017.

23. Ravi Kumar Bhukya, Satish Kumar "Investigation of A Novel Single Carrier Based Space Vector Pulse Width Modulation Techniques for Cascaded Multi level Inverter fed Induction Motor Drive", *World Journal of Modelling and Simulation (WJMS),* England, UK, Vol. 14 (2018) No. 1, pp.68-80.

24. Ravi Kumar Bhukya, Satish Kumar "Investigation of TTMC-SVPWM Strategies for DiodeClamped and Cascaded H-bridge Multi-level InverterFed Induction Motor Drive", Indonesian Journal of Electrical Engineering and Informatics (IJEEI), Vol. 5, No. 3, September 2017, pp. 248~258.

25. Ravi Kumar Bhukya, Satish Kumar "Analysis and Implementation of Unipolar PWM Strategies for Three Phase Cascade Multilevel Inverter Fed Induction Motor Drive", International Journal of Advances in Applied Sciences (IJAAS) Vol. 7, No. 3, September 2018, pp. 245~254.

26. Lokeshwar Reddy, P. Satish Kumar and M. Sushama "Design and performance analysis of Cascaded Multilevel STATCOM", *International Journal of Control theory and Applications,* Vol 10, No 16, pp. 1-11, 2017 (**ISSN :** 0974-5572) (SJR 0.17). (Scopus indexed)

27. Sridhar, P. Satish Kumarand M. Sushama "A Novel Generalized topology for Multi-level Inverter with Switched series-parallel DC Sources", *International Journal of Engineering,* IJE TRANSACTIONS C: Aspects Vol. 30, No. 6, (June 2017) 851-858. (doi: 10.5829/ije.2017.30.05b.05) (IF 1.098) (Scopus indexed), (Citation:1)

28. Sridhar, P. Satish Kumarand M. Sushama, "Phase Disposition PWM Technique for Eleven Level Cascaded Multilevel Inverter with Reduced Number of Carriers", Asian Power Electronics Journal, Vol. 11, No. 1, July 2017, pp- 1-5, (ISSN 1995-1051), (Citation:1)

29. Susheela and P. Satish Kumar, "Comparative Analysis of Carrier Based Techniques for Single phase Diode Clamped MLI and Hybrid Inverter with Reduced Components" Indonesian Journal of Electrical Engineering and Computer Science, Vol. 7, No. 3, September 2017, pp. 687-697. (ISSN:**2502-4760**, DOI: 10.11591/ijeecs.v7.i3.pp687-697) (SJR:0.23)(Scopus indexed)

30. Susheela and P. Satish Kumar, "Analysis and comparison of various pulse width modulation strategies for hybrid inverter with reduced number of components ", *International Journal of inventions in Engineering & Science Technology,* Vol 3, No 3, pp. 12-26, 2017, (ISSN: 2454-9584).

31. B.Ravi and P. Satish Kumar, "Performance analysis of modified SVPWM strategies for three phase cascaded Multilevel Inverter fed Induction motor drive", *International Journal of Power electronics and drives systems,* Vol 8, No 2, pp. 835-843, 2017 (ISSN: 2088-8694, DOI: 10.11591/ijpeds.v8i2.pp835-843)(SJR 0.25) (H index 9)(Scopus Indexed). (Citation:2)

32. Ch. Lokeshwar Reddy and P. Satish Kumar, "Implementation and performance analysis of Cascaded Multilevel Inverter using Modified SVPWM Techniques", *International Journal of Power Electronics,* Vol.9, No.3, pp.250-273, 2018 (Inderscience Journal) (Scopus indexed) (doi: 10.1504/IJPELEC.2018.10013480).

33. B. Sirisha and P. Satish Kumar, "A Simplified and Generalized SVPWM Method Including Over Modulation Zone for Seven Level Diode Clamped Inverter - FPGA Implementation", *International Journal of Power Electronics,* Vol. No. , pp- 2017 (Inderscience Journal) (Scopus indexed) Accepted).

34. Ch. Lokeshwar Reddy and P. Satish Kumar, et al., "Design and performance analysis of 7-level diode clamped Multilevel Inverter using Modified SVPWM Techniques", *International Journal of Engineering,* IJE TRANSACTIONS B: Applications Vol. 30, No. 11, (November 2017) pp1762-1770. (doi: 10.5829/ije.2017.30.11b.18), (Scopus indexed) (IF 1.098)

35. Ch. Lokeshwar Reddy and P. Satish Kumar, "Performance comparison of star connected cascaded STATCOM using different PWM Techniques", *International Journal of Power Electronics and Drives Systems (IJPEDS),* Vol 8, No 3, September 2017. pp. 1303-1319 (ISSN: 2088-8694, doi: 10.11591/ijpeds.v8.i3) (SJR 0.25) (H index 9) (Scopus indexed).

36. P. Satish Kumar, et al., "Performance Comparison of Multilevel Inverters using Modified SVPWM Techniques", *International Journal of Electrical and Computer Engineering,* Vol x, No x, pp. x, 2017. (Accepted), (Scopus indexed).

37. Ch. Lokeshwar Reddy and P. Satish Kumar, "Improvement in Performance of Cascaded Multilevel Inverter Using Triangular and Trapezoidal Triangular Multi Carrier SVPWM", *Advances In Electrical And Electronic Engineering,* Vol 14, No 05, pp.562-570, 2016, (DOI: 10.15598/aeee.v14i5.1767), (**ISSN** 1804-3119), (SJR 0.25) (Scopus indexed). (Citation: 1)

38. G. Sridhar, P. Satish Kumar and M. Sushama, "Design and Implementation of a Diagonal DC Source Multilevel Inverter Topology for Cascaded H-Bridge," Asian Power Electronics Journal, Vol. 10, No. 1, July 2016, pp- 1-5, (ISSN 1995-1051).

39. E. Sreenu and P. Satish Kumar, "Performance Analysis of Different PWM strategies for Three phase Three level Diode Clamped Multilevel Inverter", *International Journal of Industrial Electronics and Electrical Engineering,* Vol 4, Issue 12, pp.16-20, 2016. (ISSN: 2347-6982) (JIFactor 3.2) (UGC Listed).

40. Lokeshwar Reddy and P. Satish Kumar, "Modified Modulation Techniques for Cascaded Multilevel Inverter fed Induction Motor Drive", *Global Journal of Researches in Engineering : F Electrical and Electronics Engineering*, Vol 15, Issue 9, pp.17-24, 2015, (ISSN: 2249-4596),(DOI 10.17406/gjre).

41. Sridhar and P. Satish Kumar, "Phase Disposition PWM Technique for Eleven –Level Cascaded Multilevel Inverter with Reduced numbers Carriers", *TELKOMNIKA Indonesian Journal of Electrical Engineering,* Vol 15, No 1, pp.49-56, July 2015. (h-index 20, i10-index 103), (Scopus indexed), (ISSN: 2302-4046), (citation:1).

42. Satyanarayana and P. Satish Kumar, "Analysis and Design of Solar Photo Voltaic Grid Connected

Inverter", *Indonesian Journal of Electrical Engineering and Informatics*, Vol3, No. 4, 2015, pp.199-208, (ISSN 2089-3272), (DOI: 10.11591/ijeei.v3i4.174), (Scopus indexed). (Citation:3).

43. Othman M. Hussein Anssari and P. Satish Kumar, "Three Phase Single Stage Three-Thirteen level AC-DC converter", *International Journal of Electrical and Electronics Engineering Research,* 5, Issue 2, April 2015, pp.61-72, (ISSN 2250-155X), (IF: 7.89).

44. Sridhar and P. Satish Kumar, "A New General Topology for Cascaded Multilevel Inverters with Increased Number of levels Based on Diagonal DC Source H-Bridge", *Int. Journal of Advances in Electrical and Electronics Engineering*, Vol. 3, No. 3, pp.175-184, 2014, (ISSN: 2319-1112), (IF: 0.56).

45. Sirisha and P. Satish Kumar, "A Simplified Space Vector Pulse Width Modulation Method for Cascaded H-Bridge Multilevel Inverters", *International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering,* Vol. 3, Issue 12, pp. 13635- 13640, December 2014. (ISSN: 2278-8875) (IF: 6.39). (Citations:2).

46. Lokeshwar Reddy and P. Satish Kumar, "Cascaded H-bridge Multilevel Inverter Using New Phase Shifted Carrier Pulse Width Modulation Technique", *International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering,* Vol. 3, Issue 12, pp. 14001-14008, December 2014. (ISSN: 2278-8875) (IF: 6.39).

47. P. Satish Kumar, Ramu, K. Rama Krishna, "A Multilevel Synthesis Approach with Reduced Number of Switches for 99-Level Inverter", *International Science Index,* Vol. 8, No. 4, 2014, pp. 1351-1355.(dai: urn:dai:10.1999/1307-6892/12054) (SJR: 0.12).

48. Satish Kumar Peddapelli, "Recent Advances in Pulse Width Modulation Techniques and Multilevel Inverters", *International Science Index,* 8, No. 3, 2014. (doi: scholar.waset.org/1307-6892/9997993) (SJR: 0.12). (Citations:7)

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